IN THE CLAIMS

Claims 1-2 (Cancelled)

3. (Currently Amended) A method according to claim ~~1~~22, wherein said step of converting the transformed signal is performed using a biased receiver transistor network having a PFET current mirror coupled with a NFET current mirror.

4. (Cancelled) A method according to claim 1, wherein said input signal in said step of converting a noise-sensitive chip input signal originates in a first voltage domain and said intermediate signal in said multiplying step is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain.

5. (Currently Amended) A method according to claim ~~1~~22, wherein said input signal in said step of converting a noise-sensitive chip input signal originates at an off-chip signal source and is output to an on-chip signal sink included in on-chip analog circuitry.

6. (Original) A method according to claim 5, wherein said off-chip signal source is a reference clock.

7. (Currently Amended) A method according to claim ~~1~~23, wherein said converted signal in said multiplying step is input to a PLL.

8. (Original) An integrated circuit designed to reduce on-chip noise coupling, the integrated circuit comprising:

a circuit transformer capable of converting a noise sensitive input signal to an output signal having a voltage compatible with a predetermined sink voltage logic level; and

a biased receiver transistor network having a PFET current mirror coupled with a NFET current mirror, said biased receiver transistor network designed to multiply said transformer output signal to offset a mutual coupling loss of said transformer.

9. (Original) An integrated circuit according to claim 8, wherein said input signal originates in a first voltage domain and said output signal from said biased receiver transistor network is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain.

10. (Original) An integrated circuit according to claim 8, wherein said input signal originates at an off-chip signal source and is output to an on-chip signal sink included in on-chip analog circuitry.

11. (Original) An integrated circuit according to claim 10, wherein said off-chip signal source is a reference clock.

12. (Original) An integrated circuit according to claim 8, wherein said output signal from said biased receiver transistor network is input to a PLL.

13. (Original) An integrated circuit according to claim 8, wherein said transformer is a monolithic integrated transformer.

Claims 14-16 Cancelled.

17. (Currently Amended) An integrated circuit according to claim ~~14~~24, wherein said means for multiplying is a biased receiver transistor network having a PFET current mirror coupled with a NFET current mirror.

18. (Currently Amended) An integrated circuit according to claim ~~17~~24, wherein said input signal originates in a first voltage domain and said output signal from said biased receiver transistor network is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain.

Claims 19-20 Cancelled..

21. (Currently Amended) An integrated circuit according to claim ~~14~~24, wherein said output signal from said biased receiver transistor network is input to a PLL.

Please add the following new claims:

22. (New) A method of reducing electrical noise coupling to a noise-sensitive chip input signal, comprising the steps of:

providing input circuitry including a noise isolated monolithic integrated transformer;

converting a noise-sensitive chip input signal to an intermediate signal using said transformer;

converting said intermediate signal to a converted signal having a voltage level compatible with that of a predetermined logic level using auxiliary noise-isolated support circuitry; and

using said converted signal as input to intended on-chip destination circuitry.

23. (New) The method according to claim 22, further comprising the step of:

multiplying said transformer output signal to offset a mutual coupling loss of said transformer.

24. (New) An integrated circuit designed to reduce on-chip noise coupling, the integrated circuit comprising:

a monolithic integrated circuit transformer for converting a noise sensitive input signal to an output signal having a voltage compatible with a predetermined sink voltage logic level; and

means for multiplying said transformer output signal to offset a mutual coupling loss of said transformer.

CLAIM REJECTIONS UNDER 35 U.S.C. SECTION 112

On page 2 of the Current Office Action, the Examiner rejected claims 4, 7, and 14 under 35 U.S.C. Section 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 4 and 14 have been cancelled. Claim 7 has been amended to depend from newly added claim 23 which includes the previously referenced multiplying step. In light of the above, withdrawal of the rejection is respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. SECTION 102

On page 2 of the Current Office Action, the Examiner rejected claims 1, 4, 14-15, and 19-20 under 35 U.S.C. Section 102(b) as being anticipated by U.S. Patent No. 6,008,681 to Beutler et al. Claims 1, 4, 14-15, and 19-20 have been cancelled.

SUMMARY AND CONCLUSION

In view of the foregoing, withdrawal of the rejections and the allowance of the current pending claims is respectfully requested. If the Examiner feels that the pending

claims could be allowed with minor changes, the Examiner is invited to telephone the undersigned to discuss an Examiner's Amendment.

Respectfully submitted,

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